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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/473,394	12/28/1999	KAIZAD R. MISTRY	042390.P6892	9930

7590 01/23/2004

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EXAMINER
KANG, DONGHEE

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<p style="text-align: center;">Office Action Summary</p>	<p>Application No.</p> <p>09/473,394</p>	<p>Applicant(s)</p> <p>MISTRY, KAIZAD R.</p>	
	<p>Examiner</p> <p>Donghee Kang</p>	<p>Art Unit</p> <p>2811</p>	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 January 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 April 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

1. Acknowledgment is made of receipt of applicant's Information Disclosure Statement (PTO-1449) filed April 10, 2003.

Drawings

2. The drawings were received on April 10, 2003. These drawings are acceptable.

Claim Objections

3. Claims 1 & 4 are objected to because of the following informalities:

Re claim 1, line 14: the phrase "sidewalls of the recess" should be -- **-the vertical** sidewalls of the recess-- .

Re claim 4, line 14: the phrase "sidewalls of the recess" should be - **-the tapered** sidewalls of the recess-- . Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims **1-3** are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (US 6,303,448).

Regarding claim **1**, Chang et al. disclose a field effect transistor, comprising (Fig.6):

a substrate (10) having a recess in a surface thereof; the recess having a bottom portion and substantially vertical sidewalls; a gate dielectric layer (62) disposed superjacent the bottom portion of the recess and adjacent the substantially vertical sidewalls; a gate electrode (64A) completely overlying the gate dielectric layer; and source/drain terminals (70) disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls, said gate electrode extending to a less shallow depth within said substrate than a depth at which the source/drain terminals are disposed; wherein the source/drain terminals comprises an extension (LDD,66) which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, an entire innermost side of the extension is adjacent to the vertical sidewalls of the recess, a portion of the gate dielectric layer overlying an innermost portion of the extension.

The word "adjacent" is a broad term, which means not distant or nearby (Merriam-Webster's Collegiate Dictionary). Figure 6 clearly shows that the entire innermost side of the extension is adjacent to the sidewalls of the recess.

Regarding claim **2**, Chang et al. disclose the transistor further comprising a portion of the gate electrode that overlies the innermost portion of the extension.

Regarding claim **3**, Chang et al. disclose that the gate electrode conforms to a recessed channel.

6. Claims **4-6** are rejected under 35 U.S.C. 102(a) as being anticipated by Gardner et al. (US 5,918,134).

Regarding claim **4**, Gardner et al. disclose a field effect transistor, comprising (Fig.10):

a substrate (102) having a recess in a surface thereof; the recess having a bottom portion and tapered sidewalls, the tapered sidewall surface forming an obtuse angle with respect to the bottom portions of the recess; a gate dielectric layer (132) disposed superjacent the bottom portion of the recess and adjacent the tapered sidewalls; a gate electrode (134) completely overlying the gate dielectric layer; and source/drain terminals (140a) disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls; wherein the source/drain terminals comprises an extension (130) which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, an entire innermost side of the extension is adjacent to sidewalls of the recess, a portion of the gate dielectric layer overlying an innermost portion of the extension.

The word "adjacent" is a broad term, which means not distant or nearby (Merriam-Webster's Collegiate Dictionary). Figure 10 clearly shows that the entire innermost side of the extension is adjacent to the tapered sidewalls of the recess.

Regarding claim **5**, Gardner et al. disclose that a portion of the gate electrode overlies an innermost portion of extension.

Regarding claim **6**, Gardner et al. discloses that the gate electrode conforms to a recessed channel.

7. Claims **7-9** are rejected under 35 U.S.C. 102(b) as being anticipated by Ahn et al. (US 5,342,796).

Regarding claim **7**, Ahn et al. disclose a field effect transistor, comprising (Fig.9): a substrate (1) having a recess in a surface thereof, the recess having a curvilinear shape; a gate dielectric layer (7) disposed superjacent the curvilinear recess; a gate electrode (9) completely overlying the gate dielectric layer (see Fig.7); and source/drain terminals (13) disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls, wherein the source/drain terminals comprises an extension (11) which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the curvilinear sides of the recess, a portion of the gate dielectric layer overlaying an innermost portion of the extension.

Regarding claim **8**, Ahn et al. disclose that a portion of the gate electrode overlies an innermost portion of the source/drain extension.

Regarding claim **9**, Ahn et al. disclose that the gate electrode conforms to a recessed channel.

Response to Arguments

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8. Applicant's arguments filed 21 October 2002 have been fully considered but they are not persuasive.

Applicant argues that Chang et al. do not teach the entire innermost portions of the extension being adjacent to the vertical sidewalls of the recess. The word "adjacent" is a broad term, which means not distant or nearby (Merriam-Webster's Collegiate Dictionary). Figure 6 clearly shows that the entire innermost side of the extension is adjacent to the vertical sidewalls of the recess. The innermost side of the extension does not have to be in contact to the sidewalls. Therefore, the 102 (e) rejection anticipates each and every element as set forth in claim 1.

Applicant argues that Gardner does not teach the entire innermost portion of the extension being adjacent to the tapered sidewalls of the recess. The word "adjacent" is a broad term, which means not distant or nearby (Merriam-Webster's Collegiate Dictionary). Figure 10 clearly shows that the entire innermost side of the extension is adjacent to the tapered sidewalls of the recess. The innermost side of the extension does not have to be in contact to the tapered sidewalls. Therefore, the 102(a) rejection anticipates each and every element as set forth in claim 4.

Applicant argues that Ahn does not teach the gate electrode completely overlying the gate dielectric layer because there is portion of the oxide film that surrounds the vertical sidewalls of the electrode 9. This is not convincing. The side oxide layer is not gate dielectric layer. It is acknowledged in the art that sidewall layer or spacer layer. The

sidewall/spacer layers have different function compared to gate dielectric layer.

Therefore, the gate electrode 9 is completely overlying the gate dielectric layer.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 703-305-9147. The examiner can normally be reached on Maxiflex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 703-308-1690. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



Donghee Kang
Examiner
Art Unit 2811

dhk